1. Examples handout questions 21, 22, 23, 24, 25

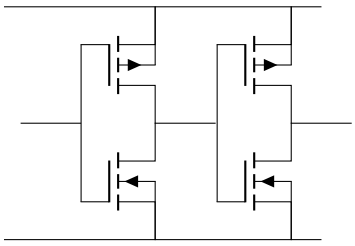
2. The lecture notes show an example of a CMOS NAND gate with two inputs. However, many of the boolean functions discussed in lecture and in the assignments require logic gates with 3 inputs.

   (a) Draw a CMOS NAND gate with three inputs.

   (b) Draw a NMOS logic NOR gate with three inputs.

   (c) The resistance of a MOSFET that is conducting is small but non-zero. For the NAND and NOR gates you drew above, identify what parts of the circuit will increase in resistance as the number of inputs increases. Describe how performance might suffer in a NAND or NOR gate with a very large number of inputs.

3. When linking up logic gates to form a boolean circuit, the output of a logic gate (e.g., NOT gate, NAND gate, etc.) in CMOS logic connects to the gate terminals of the MOSFETs of the next logic gate in the circuit. For example, in the circuit below, notice how the output of the first CMOS inverter splits up and connects to the gates of the two MOSFETs that form the second CMOS inverter.



   (a) The gate terminal of each MOSFET is said to behave a lot like a capacitor. Explain why this is the case using a diagram of the structure of a MOSFET. Hint: Consider what parts of the MOSFET are conductors and insulators.

   (b) If the output of a logic gate gets split up and connects to many downstream gates it is said to have a *high fanout*. In this situation, the downstream MOSFETs combine to form what is effectively a very big capacitor at the output of the logic gate. What impact does an increased capacitance have on the switching speed of the output?