1. Examples handout questions 21, 22, 23, 24, 25
2. The lecture notes show an example of a CMOS NAND gate with two inputs. However, many of the boolean functions discussed in lecture and in the assignments require logic gates with 3 inputs.
   (a) Draw a CMOS NAND gate with three inputs.
   (b) Draw a NMOS logic NOR gate with three inputs.
3. The *fanout* of a logic gate is the number of downstream logic gate inputs to which the gate output connects. A gate with an output that connects to many different inputs is said to have a *high fanout*. What practical physical limitations restricts the size of the fanout?